Semiconductor packaging, assembly and test in Europe

By Steffen Kroehnert [NANIUM S.A.]

The advance of semiconductor technology has slowly been moving away from developments at the front end of the process line towards improving both cost and performance of the chip packaging assembly and test processes at the back end of the line. So much so, that advanced packaging capability, such as TSV and 3D IC, has now become a significant driver for the whole of the industry.

High-volume manufacturing moved to Asia

It is estimated that some 80-90% of the semiconductor, assembly and test industry has moved to Asia during the last three decades (**Table 1**). In Europe, even the major IDMs such as, Infineon Technologies AG, STMicroelectronics, NXP and Robert Bosch GmbH, moved the majority of their packaging, assembly and test manufacturing to Asia. However, Europe continues to be strong in the design, development and production of semiconductor manufacturing equipment related to packaging, assembly and test and has strong R&D supported by academic and institutes such as, Fraunhofer, CEA-Leti, and imec. Yet production packaging, assembly and test remains mainly for low- and mid-size volume sensitive, and more complex products. With few exceptions, high-volume manufacturing (HVM) of consumer and commodity products was moved mainly to Asia, generally for cost reasons. The result, which has been learned during the last few years, is that R&D without a certain level of manufacturing "onsite" in Europe does not work long-term, as the manufacturability feedback is missing. The newly established pilot lines might help, but they do not solve the problem.

The advanced packaging in Europe today concentrates mainly on system-in-package (SiP), wafer-level packaging (WLP), MEMs and sensor packaging, the packaging of photovoltaics and optoelectronic devices. It is clearly application driven and crucially serves, in many cases, quite attractive niche markets such as, industrial, security, medical, defense, aerospace and aeronautics by offering packages for hermetically sealed, high-reliability and advanced designs. Inherently, this means "low-volume" at typically "high-value." The residual European packaging process can be summarized to be the following steps: application design (ASP), prototype, pre-production, outsource production, which, simplified, means export of designs and know-how. But there is now a change underway.

Sector	Innovation	Design	Manufacturing	Utilization
Aerospace	USA	Europe	Europe	USA
Automotive	Europe	Europe	Asia	Europe
Broadcast	Europe	USA	Asia	Europe
Communications	Europe	USA	USA	USA
Computing	USA	USA	Asia	USA
Consumer	Asia	Asia	Asia	Asia
Industrial	Europe	USA	Asia	Asia
Medical	USA	Europe	Europe	Europe
Military	Europe	USA	Europe	USA
Security	Europe	USA	USA	USA

Table 1: Market generators: Where innovation, design, manufacturing and main utilization happen today, for different markets and applications. Source: PandA 2010

Semiconductor packaging is becoming fairly more complex

Historically, semiconductor packaging was seen as a post-innovative process step to put some ceramic or plastic around the chip and get either metal leads, solder balls out, or simply larger contact pads exposed to the outside in order bring the chip into the component tester and later solder it to a PCB. The package was not supposed to negatively influence the electrical and thermal performance of the product too much, and it was not supposed to be a cost adder, as it was not perceived to bring added value to the product. Those days are definitely gone.

Today, simple single-chip solutions are being pushed more and more aside in the advanced packaging area by smart system approaches (**Figure 1**). High-speed requirements are driving needs for low package parasitics, mobile applications are pushing the reduction of form factor—mainly height and thermal dissipation challenges need to be solved at the system level. This has slowed down the system-on-chip (SoC) euphoria, leading to partial reduction with integration of SoC moving to the heterogeneous integration of several active chips and passives in the package. This so called system-in-package (SiP) is the reality. This is also known as the "More-than-Moore" versus "More Moore," which is driven by the continued reduction of the wafer processing technology nodes for SoC.

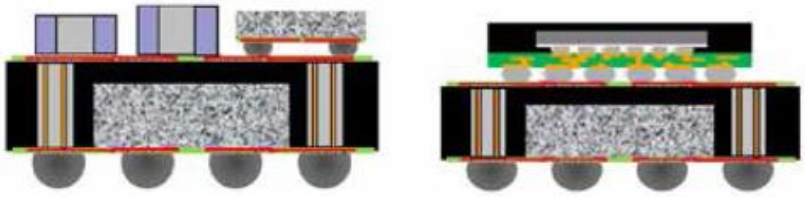


Figure 1: Advanced packaging is getting more complex. Thin package-on-package solutions under 1.0mm total package height using fan-out WLP/eWLB-based bottom package with fan-in WLCSP, flip-chip in package and SMT as top package for mobile applications. (Source: NANIUM 2013)

Packaging is coming back to Europe

The package is now very much an integral part of the product and its performance now adds significant value to the product. This is, at last, being acknowledged by the chip designers and system architects, who now have to move closer together to co-design and co-develop new system solutions.

What are the reasons for semiconductor packaging, assembly and test coming back to Europe? First of all, there are the more complex system needs, requiring new technologies and a collaborative approach through the entire supply chain. Also, increasing costs in Asia are making packaging in Europe viable and attractive again. Industry players, especially medium and small size companies, are not only looking at the cost figures, but are also looking at other considerations that can be better provided by the European companies. These are: high level engineering capability, an experienced and knowledgable workforce right down to the operator level, the high commitment of each employee, low work force churn rates, easy communication, little or no time differences, insignificant costs for travel to the service provider, no real need to install resident engineers onsite and, not the least important – the IP protection.

European industrial strategy for micro/nanoelectronics

The "EU 10/100/20" Factsheet summarizes the cornerstones: on May, 23, 2013, Mrs. Neelie Kroes, European Commission Vice-President, launched an ambitious new strategy to get 20% of global semiconductor manufacturing market back to Europe by 2020. This will be achieved by an unprecedented public/private investment partnership: €10 Billion public/private funding for research and innovation, plus € 100 Billion from industry for manufacturing. This strategy is more than just a vision, it is a major opportunity to participate in large-scale investment projects. The strategy is also important, as this is the first clear statement by public

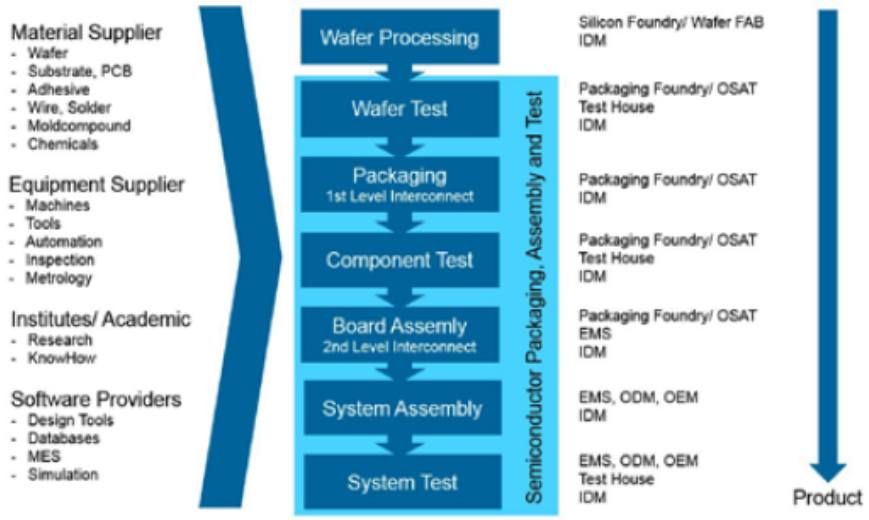


Figure 2: Semiconductor supply chain: the main focus today is still on wafer processing, but the entire supply chain needs to be considered, including semiconductor packaging, assembly and test.

authorities in Europe that they are committed to reinforcing semiconductor manufacturing-related investment in Europe.

The strategy will, along with other measures, reverse Europe's declining trend in micro- and nanoelectronics manufacturing, focus on Europe's strength, and support cross-border cooperation to create critical mass in knowledge and financing, investments in "More-than-Moore" on 200mm and 300mm, "More Moore" on 300mm, and the 450mm transition.

The strategy is targeting the integration of leading manufacturers, research centers and small and medium-sized enterprises (SMEs) into the value chain by offering access to the latest technology and state-of-the-art research facilities, and the entire supply and innovation chain (research, design, materials, equipment, manufacturing processes, device makers) (**Figure 2**). Furthermore, the strategy will focus on European clusters of excellence (Dresden, Grenoble, Eindhoven/ Leuven) and there will be cooperation with specialized clusters elsewhere. Europe, however, does not have an existing specialized European packaging, assembly and test cluster of excellence yet, especially when talking about manufacturing. So the European players in this arena should consider the formation of such a cluster.

By estimating that just 10% of the supply chain is related to packaging, assembly and test manufacturing services, the investments in this area, driven by the EU 10/100/20 initiative will be around €11 Billion, of which €1 Billion is publically/privately funded, and €10 Billion is invested by the industry. Looking at the packaging, assembly and test industry that remains in Europe, it is obvious that support from the large European IDM and/or from the large packaging foundries and outsourced semiconductor assembly and test services (OSATS) such as, ASE Group, Amkor Technology, STATS ChipPAC, SPIL and UTAC Group, would be welcome to invest in Europe to build long-term manufacturing capabilities and capacities and bring manufacturing jobs to Europe.

Positioning of European semiconductor packaging, assembly and test

Following an initiative of the largest European packaging foundry/OSAT, NANIUM S.A. in Portugal, together with specialized consultancy PandA (Packaging and Assembly) Europe, an industry interest group called "ESPAT" (European Semiconductor Packaging, Assembly and Test) has been started. ESPAT intends to work closely with the European branches of the industry associations, including SEMI (Semiconductor Equipment and Materials International) and its Advanced Packaging Conference (APC) Committee, the GSA (Global Semiconductor Alliance), and IMAPS-Europe.

Preliminary: European semiconductor packaging, assembly and test

The ESPAT initiative is set down as follows:

Scope. European semiconductor packaging, assembly and test manufacturing companies of all types and sizes are included:

- High, medium and small volume manufacturing sites;
- Manufacturers of prototypes, samples and small series in lab scale;
- Engineering and manufacturing services of equipment suppliers;
- Packaging, assembly and test activities of European IDMs in Europe; and
- Companies interested in investing in packaging, assembly and test manufacturing in Europe).

Objectives. The objectives are several:

- To promote the increasingly important role of ESPAT in the semiconductor supply chain:
  - More-than-Moore, heterogeneous system integration, system-in-package; and
  - Chip-package-board co-design and co-development.
- To build-up a platform for European semiconductor packaging, assembly and test manufacturing players;
- To give them a voice at the European Commission in Brussels; and
- To build European strength in assembly and test by proposing cooperative efforts to complement and develop capabilities.

Strategy. The strategy is two-fold:

- Influence and participate in "EU 10/100/20" Industry Strategy/ Horizon2020 funded projects (when considering the entire semiconductor supply chain, ESPAT makes up an estimated 10% of this supply chain, so the funding should be appropriate); and
- Build-up manufacturing capability and capacity in Europe for pilot lines and beyond.

Tasks. First of all, the new ESPAT Industry Interest Group will interact

with its members and partners to analyze what is available in terms of semiconductor packaging, assembly and test manufacturing in Europe, and what are the strengths. The aim is to create and make available a "Packaging, Assembly and Test Manufacturing Service Provider in Europe Directory" showing who is doing what, and showcase and promote those services in a consolidated way to the customers.

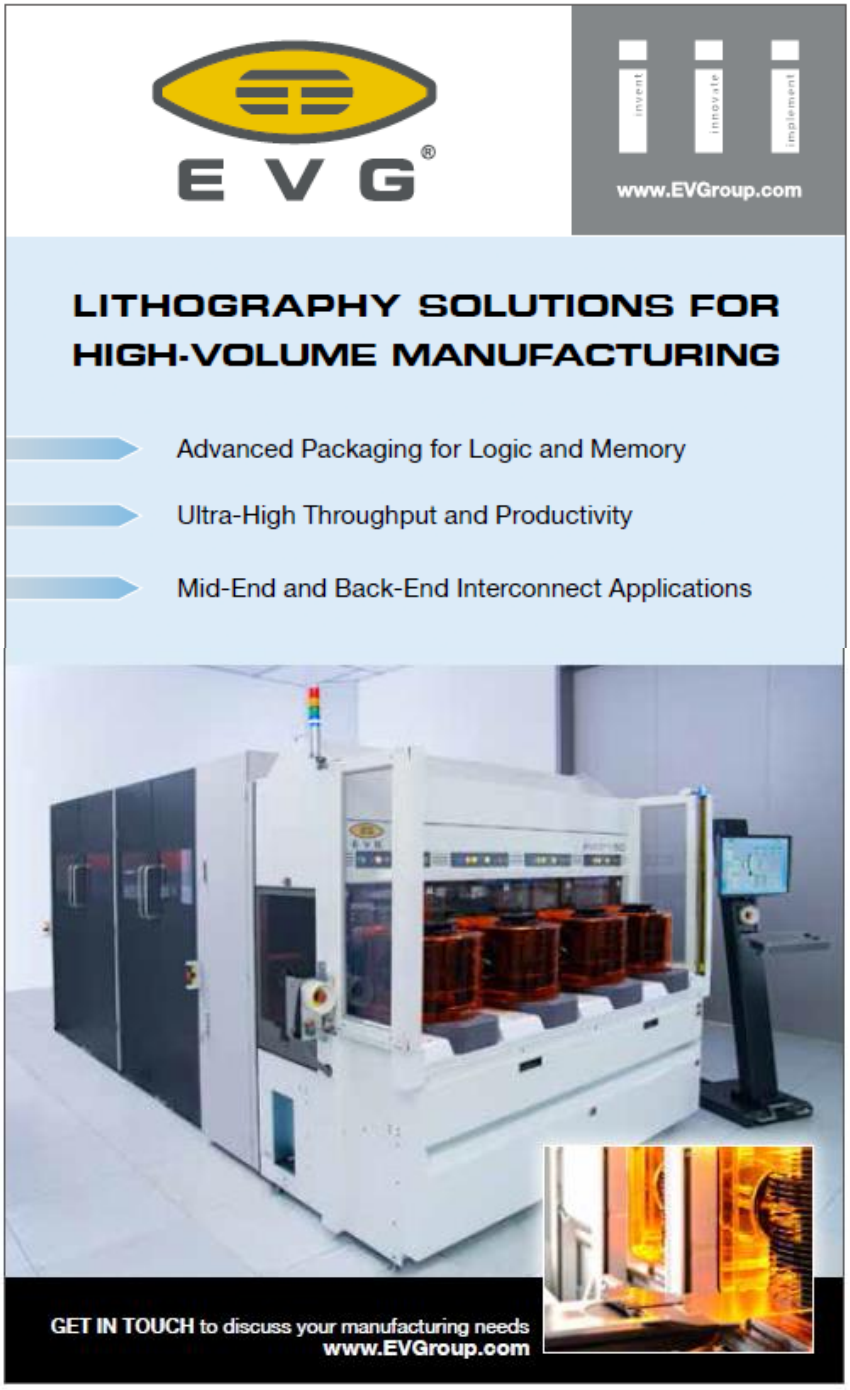
The next step is to analyze the gaps by comparing current capabilities and capacities with international package technology roadmaps provided by recognized market research institutes and associations and customer roadmaps. The gaps will need to be made known to the decision makers in the European Commission. We will discuss together what is needed to close those gaps. The themes for funded project calls have to been influenced in a way to support those topics. In order to close those gaps, we will need to build-up cooperative efforts, targeting ways to motivate smaller and mid-sized manufacturing companies to participate in funded cooperative projects in order to benefit from the new industry strategy. It is essential for success that we ensure the creation of a "win-win" situation for all participating packaging, assembly and test manufacturing companies.

Mid-term, it is planned to convert the ESPAT Industry Interest Group into an officially registered Special Interest Group (SIG), possibly inside the SEMI organization, in order to run the necessary advocacy work and underline the importance of this part of the semiconductor supply chain.

It is planned to have a first face-to-face meeting of the ESPAT Industry Interest Group at Semicon Europa 2014 from October, 7-9, 2014, in Grenoble, France.

Additionally, during the Advanced Packaging Conference (APC), held in conjunction with Semicon Europa 2014, a panel discussion "Packaging in Europe – High Value, Low Volume?!" is planned. This will be the first opportunity to showcase ESPAT European packaging, assembly and test capabilities, capacities, and plans in a consolidated way.

Finally, during Q1/2015, a SEMI Europe Networking Day is planned at NANIUM in Vila do Conde, Portugal. At this event, ESPAT will again showcase "European Packaging, Assembly and Test" and bring the European manufacturing supply chain together with policies, associations, customers, and suppliers.

Biography

Steffen Kroehnert received his master's degree in Electrical Engineering and Microsystems Technologies from the Technical U. of Chemnitz, Germany, and is Director of Technology at NANIUM S.A.; he is also a co-chair of the SEMI Europe APC Committee; email steffen.kroehnert@nanium.com; and/or Andy Longford, Managing Director, PandA Europe, and a co-chair of SEMI Europe APC Committee; email andy@pandaeurope.com